WHAT IS CLAIMED IS:

1. A matrix switch circuit, comprising:

total (n x m) pieces of m-to-1 selectors to which one frame where n (n: positive integer) pieces of unit data are serially arrayed is input by m (m: positive integer) pieces in parallel, from which predetermined one frame specified in an address is output and which are divided into m pieces of groups each of which includes n pieces;

(n x m) pieces of selecting circuits that respectively receive the output of the m-to-1 selector and respectively select specific unit data specified in an address in one frame;

m pieces of n-to-1 selectors that respectively receive data output from n pieces of selecting circuits, respectively forms and outputs one frame; and

a control circuit that sends a control signal to the selecting circuits and the n-to-1 selectors.

2. A matrix switch circuit, comprising:

total (n x m) pieces of m-to-1 selectors to which one frame where n (n: positive integer) pieces of unit data are serially arrayed is input by m (m: positive integer) pieces in parallel, from which predetermined one frame specified in an address is output and which are divided into m pieces of groups each of which includes n pieces;

(n x m) pieces of selecting circuits that respectively receive the output of the m-to-1 selector and respectively selects specific unit data specified in an address in one frame;

m pieces of n-to-1 selectors that respectively receive data output from n pieces of selecting circuits, respectively forms and outputs one frame; and

a control circuit that sends a control signal to the selecting circuits and the n-to-1 selectors, wherein:

data input to the matrix switch circuit is p (p: positive integer)-bit parallel data; and

(p x n x m) pieces of m-to-1 selectors are arranged, (p x m) pieces of n-to-1 selectors are arranged and (p x m) pieces of input/output lines are arranged.

3. A matrix switch circuit according to Claim 1, wherein:

data input to the matrix switch circuit is p (p: positive integer)-bit serial data.

4. A matrix switch circuit according to Claim 1, wherein:

the selecting circuit is provided with first and second circuits to which data output from the m-to-1 selector is written and from which the written data is read and a switching circuit that switches these circuits.

5. A matrix switch circuit according to Claim 4, wherein:

the first and second circuits are a flip-flop circuit.

6. A matrix switch circuit according to Claim 4,

wherein:

the first and second circuits are arranged in parallel with the m-to-1 selector.

7. A matrix switch circuit according to Claim 4, wherein:

the first and second circuits are cascaded for the m-to-1 selector.

8. A matrix switch circuit according to Claim 7, wherein:

the first circuit on the side of the m-to-1 selector is a reset-set flip-flop circuit.

9. A matrix switch circuit according to Claim 1, wherein:

the unit data is a synchronous transfer signal (STS)-1.

10. A matrix switch circuit according to Claim 2, wherein:

the unit data is a synchronous transfer signal (STS)-1.

11. A matrix switch circuit according to Claim 1, wherein:

the m-to-1 selector comprises:

m pieces of 2-input AND gates;

one m-input OR gate connected to the m pieces of 2-input AND gates; and

a decoder to which address information is input, wherein:

a data input line and an output line of the decoder are connected to each 2-input AND gate; and

the m-input OR gate outputs the output of predetermined one 2-input AND gate.

12. A matrix switch circuit according to Claim 11, wherein:

data input to the m-to-1 selector is p (p: positive integer)-bit parallel data;

(p x m) pieces of 2-input AND gates are arranged; and

p pieces of m-input OR gates are arranged.

13. A matrix switch circuit according to Claim 1, wherein:

the m-to-1 selector comprises:

m pieces of 2-input AND gates;

q (q < m) pieces of AND gates;

q pieces of selectors; and

a q-input OR gate, wherein:

the m pieces of 2-input AND gates are divided into q pieces of groups;

a data input line and an output line of the AND gate are connected to each 2-input AND gate;

the output of the 2-input AND gate in each group is input to one selector;

the output of q pieces of selectors is input to the OR gate; and

address information is input to the q pieces of AND gates and the q pieces of selectors.

14. A matrix switch circuit according to Claim 13, wherein:

data input/output to/from the m-to-1 selector is p (p: positive integer)-bit parallel data;

(p x m) pieces of 2-input AND gates are arranged;

(p x q) pieces of AND gates are arranged:

(p x q) pieces of selectors are arranged; and

p pieces of q-input OR gates are arranged.

15. A matrix switch circuit according to Claim 1, wherein:

at least one m-to-1 selector is formed by a field programmable gate array.

16. A matrix switch circuit according to Claim 2, wherein:

at least one m-to-1 selector is formed by a field programmable gate array.

17. A matrix switch circuit according to Claim 1, comprising:

a 2-input AND gate that sends a signal to each m-to-1 selector, wherein:

unit data is input to one input terminal of the 2-input AND gate and a signal output from the selecting circuit is input

to the other terminal.

18. A matrix switch circuit according to Claim 1, comprising:

a 2-input AND gate that sends a signal to each m-to-1 selector, wherein:

unit data is input to one input terminal of the 2-input AND gate and the output of a decoder circuit that decodes and outputs address information is input to the other terminal.